**Hint:**

In the excel files, the DATA order is as follows:

VIN (for both VINP and VINN), VB1, C0, R0, L1, W1, L2, W2, L3, W3, L4, W4, L5, W5, Power, Gain, BW\_3dB, UGB, PM, GM.

The units for them are listed below: **V**: (mV), **C**: (pF), **R**: (KOhm), **L**: (nm), **W**: (um), **Power**: (W), **Gain**: (dB), **BW\_3dB**: (Hz), **UGB**: (Hz), **PM**: (degree), **GM**: (dB)

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| --- | --- |
| Prompt | Completion |
| Determine the resistor and capacitor values, the sizing of MOSFET transistors, and the biasing voltages (i.e., R0, C0, L1, W1, L2, W2, L3, W3, L4, W4, L5, W5, VIN (for both VINP and VINN), VB1) for the provided two-stage amplifier using TSMC 65nm CMOS technology to achieve the specified amplifier performance metrics. The amplifier consists of 5 MOSFET transistors in the first stage and 2 MOSFET transistors in the second stage, along with a capacitor and a resistor as a feedback connection (Miller) at the second stage NMOS transistor (M6).  **First Stage: Input Transistors:** M1, M2 (PMOS): Differential input transistors with the same sizing (L1, W1). Differential input signal applied.  **Current Mirror & Load:** M3, M4 (NMOS): Current mirror and load transistors with the same sizing (L3, W3).  **Biasing Transistor:** M5 (PMOS): Current source transistor with sizing (L2, W2) and gate voltage (VB1).  **Second Stage:** **Biasing Transistor:** M7 (PMOS): Biasing transistor with sizing (L5, W5) and gate voltage (VB1).  **Amplifying Transistor:** M6 (NMOS): Connected with a resistor (R0) in series with a capacitor (C0) as feedback. Sizing (W4, L4) controls the gain of the second stage.  **Netlist:** **MOSFET Transistors:**   * + M1 pch net3 VINP net2 VDD L1 W1   + M2 pch net1 VINN net2 VDD L1 W1   + M5 pch net2 VB1 VDD VDD L2 W2   + M3 nch net3 net1 GND GND L3 W3   + M4 nch net1 net1 GND GND L3 W3   + M6 nch VOUT net3 GND GND L4 W4   + M7 pch VOUT VB1 VDD VDD L5 W5   **Capacitor:**   * + C0 net3 net4 C0\_value   **Resistor:**   * + R0 net4 VOUT R0\_value   **Netlist Column Explanation:**  Component Name (M for MOSFET, C for Capacitor, R for Resistor)  **For transistors:**Type (pch for PMOS, nch for NMOS), Drain Net Name, Gate Net Name, Source Net Name, Bulk Net Name, Length (L) of the Transistor, Width (W) of the Transistor  **For resistor and capacitor:** One terminal net name, Other terminal net name, Capacitor or Resistor Value  **Biasing Voltages:** VINP, VINN, VB1.  **Performance Metrics:** Power: Column\_O, Gain: Column\_P, 3dB Bandwidth (BW\_3dB): Column\_Q, Unity Gain Bandwidth (UGB): Column\_R, Phase Margin (PM): Column\_S, Gain Margin (GM): Column\_T | To achieve the given performance metrics with the provided amplifier netlist, you can use the following values in the netlist:   * + M1 pch net3 VINP net2 VDD L1=Column\_E W1=Column\_F   + M2 pch net1 VINN net2 VDD L1=Column\_E W1=Column\_F   + M5 pch net2 VB1 VDD VDD L2=Column\_G W2=Column\_H   + M3 nch net3 net1 GND GND L3=Column\_I W3=Column\_J   + M4 nch net1 net1 GND GND L3=Column\_I W3=Column\_J   + M6 nch VOUT net3 GND GND L4=Column\_K W4=Column\_L   + M7 pch VOUT VB1 VDD VDD L5=Column\_M W5=Column\_N   + C0 net3 net4 C0\_value=Column\_C   + R0 net4 VOUT R0\_value=Column\_D   And with biasing voltages of VINP=VINN=VIN= Column\_A, VB1= Column\_B. |